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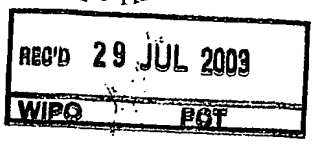

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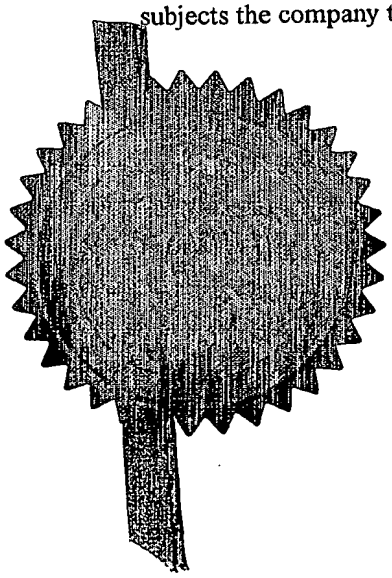

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GROENEWOUDSEWEG 1
5621 BA EINDHOVEN
THE NETHERLANDS

Patents ADP Number (*if you know it*) 7586605002

If the applicant is a corporate body, give the country/state of its incorporation — THE NETHERLANDS

4. Title of the invention — ELECTRONIC DEVICES AND THEIR MANUFACTURE

5. Name of your agent (*if you have one*) — DANIEL SHARROCK

"Address for service" in the United Kingdom to which all correspondence should be sent (*including the postcode*)

Philips Intellectual Property & Standards
Cross Oak Lane
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Patents ADP number (*if you know it*) 8209363002

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Country	Priority Application number	Date of filing

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application

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Signature D. J. Sharrock Date 5 July 2002
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DESCRIPTION

ELECTRONIC DEVICES AND THEIR MANUFACTURE

This invention relates to a electronic devices comprising polycrystalline semiconductor material and methods for manufacturing the material and such devices.

The high carrier mobility of polycrystalline silicon (poly-Si) relative to amorphous silicon (a-Si) makes it an attractive material for use in large area electronic devices such as active matrix liquid crystal displays (AMLCDs), active matrix polymer LED displays (AMPLEDs), solar cells and image sensors. Conventionally, poly-Si films used for example in thin film transistors (TFTs) have been manufactured by solid phase crystallisation (SPC). This involves depositing an a-Si film on an insulating substrate and crystallising the a-Si film by exposing it to a high temperature for a prolonged period of time, that is typically a temperature in excess of 600°C for up to 24 hours.

As an alternative, US-A-5147826 discloses a lower temperature method of crystallising an a-Si film. The method comprises the steps of depositing a thin film of metal atoms (of nickel, for example) on the a-Si film and annealing the film. The metal stimulates crystal growth at temperatures below 600°C and also provides more rapid crystal growth than would otherwise occur. For example, a typical anneal using the method of US-A-5147826 might be at around 550°C for 10 hours. This represents an improvement over prior methods for at least two reasons: first, it enables low cost non-alkali glass substrates such as borosilicate to be used which would normally suffer glass compaction and warp at temperatures of 600°C or more; and secondly, as the anneal duration is reduced, the manufacturing throughput rate is increased and therefore the associated manufacturing cost may be reduced. The contents of US-A-5147826 are incorporated herein by reference.

More recently, the production of poly-Si using a laser annealing process has been developed and widely adopted commercially. However, this process is relatively slow in that a narrow laser beam is gradually scanned across a

substrate irradiating each portion of the surface with several shots, and it is also expensive to implement and maintain. The annealing step in the process of US-A-5147826 can be carried out as a relatively simple batch process in a furnace allowing higher throughput.

TFTs manufactured using the techniques of US-A-5147826 have been hampered by the problem of relatively high leakage currents in their "off" state, making them unsuitable for use in applications such as AMLCDs. This flaw leads to inadequate image retention by the AMLCD.

Typically, in an existing poly-Si AMLCD, an acceptable value of the TFT minimum leakage current (that is, the minimum value of its leakage current across its normal operating range of gate voltage) is around 10pA or lower at a source-drain voltage of 5V. That is, it is undesirable for the TFT off-current to exceed this value during normal operation of the display as otherwise the current leakage will lead to unacceptable degradation of the display output. This threshold may vary somewhat depending on the characteristics of the picture element associated with the TFT. For a TFT with a channel width of say 4μm, a leakage current of 10pA equates to 2.5×10^{-12} A/μm. (It will be appreciated that A/μm in the context of TFTs in this specification means amperes per μm of channel width of a TFT).

The paper entitled "A High-Performance Polycrystalline Silicon Thin-Film Transistor Using Metal-Induced Crystallisation with Ni Solution", Jpn. J. Appl. Phys. Vol. 37 (1998) pp7193-7197 by Sooyoung Yoon et al discloses further developments in the techniques of US-A-5147826. A 100nm thick a-Si film on a substrate is crystallised by dipping it in a Ni absorption solution and then annealing the film at 500°C for 20 hours. The Ni concentration in the resulting poly-Si is 1.2×10^{18} atoms/cm^3. The off-state leakage current of a TFT with a channel of poly-Si formed using this process was found to be 2.7×10^{-11} A/μm at a drain voltage of 5V, an order of magnitude greater than the threshold referred to above.

It is an object of the present invention to form electronic devices comprising polycrystalline semiconductor material in a more cost effective manner.

The present invention provides a TFT comprising a channel defined in a layer of polycrystalline semiconductor material produced by crystallising amorphous semiconductor material using metal atoms to accelerate the crystallisation process, wherein the polycrystalline semiconductor material includes an average concentration of metal atoms in the range $1.3x10^{18}$ to $7.5x10^{18}$ atoms/cm^3. Using this metal concentration, the inventors have been able to make TFTs having improved leakage current characteristics. In particular, the TFTs exhibit a minimum leakage current of around $2.5x10^{-12}$ A/μm or less at a source-drain voltage of 5V. A TFT with this property may be suitable for use as a switching element in an AMLCD or AMPLED without the TFT off-state leakage current degrading the display performance to an unacceptable extent.

The inventors have unexpectedly found that the use of metal atoms in the concentration range referred to above enables polycrystalline semiconductor TFTs to be formed with the leakage properties defined above with an annealing process of duration significantly less that previously thought necessary. Whilst an annealing time of 20 hours at a temperature of around 550°C achieves the desired properties, it has also been realised that the metal concentrations disclosed herein enable this time to be reduced to 10 hours or even 8 hours or less at a temperature of 600°C or less. This leads to substantial productivity and efficiency increases in the manufacturing process.

Preferably, the average concentration of metal atoms in the polycrystalline semiconductor material is greater than $1.9x10^{18}$ atoms/cm^3 and/or less than $5x10^{18}$ atoms/cm^3.

In a preferred embodiment, the average concentration of metal atoms is around $2.5x10^{18}$ atoms/cm^3.

Preferably, the TFT has a low-doped drain (LDD) structure. This may increase the range of gate voltage over which the minimum leakage current is substantially achieved.

The invention further provides a method of manufacturing such a device including the steps of:

(a) depositing amorphous semiconductor material on a substrate;

(b) adding metal atoms to the semiconductor material at an average concentration therein in the range $1.3x10^{18}$ to $4x10^{18}$ atoms/cm^3, the metal atoms being suitable for accelerating the crystallisation of amorphous semiconductor material; and

(c) annealing the amorphous semiconductor material to form polycrystalline semiconductor material.

Furthermore, it has been found that the application of an electric field to a substrate during the annealing step may further accelerate the process, reducing its duration.

It will be appreciated that various metal atoms may be used in the process of the invention. One or more elements selected from the group consisting of Ni, Cr, Co, Pd, Pt, Cu, Ag, Au, In, Sn, Pb, As, and Sb may be employed. More preferably, one or more elements from the group Ni, Co and Pd are used.

References herein to addition of metal atoms include the metal in elemental form or a compound including atoms of the metal.

Ion implantation is preferably used to dose amorphous semiconductor material with metal in the process of the invention as it affords precise control over dosage, uniformity and ion depth. Nevertheless, other methods may be employed for this purpose. For example, the metal atoms may be applied to the amorphous semiconductor material in a solution, typically by a spin-coating process. Other processes include sputtering or sol-gel coating a layer of nickel, and the use of a nickel precursor during the amorphous semiconductor material CVD process.

Embodiments of the invention will now be described by way of example with reference to the accompanying schematic drawings wherein:

Figure 1 shows the metal implantation step of a process in accordance with an embodiment of the invention;

Figure 2 shows the relationship between nickel concentration and depth within a semiconductor film for different doping processes; and

Figure 3 shows a poly-Si TFT formed using a process embodying the invention.

It should be noted that the Figures are diagrammatic and not drawn to scale. Relative dimensions and proportions of parts of these Figures have been shown exaggerated or reduced in size, for the sake of clarity and convenience in the drawings.

A process embodying the invention will be described with reference to Figure 1. It shows a layer of a-Si 2 which has been deposited on a glass substrate 4. The layer may typically be 40nm thick and formed using plasma enhanced chemical vapour deposition (PECVD), for example.

An areal density of nickel of around $1x10^{13}$ atoms/cm^2 is then implanted into the a-Si layer (this step is represented in Figure 1 by arrows 6) at an implantation energy typically of 20keV. Energies of up to 30keV have been successfully used with layers of this thickness to create TFTs with the desired leakage characteristics. It can be seen that the average concentration of nickel atoms in the 40nm thick a-Si layer resulting from this dose is therefore around $2.5x10^{18}$ atoms/cm^3.

Typical nickel dose profiles in the a-Si layer are illustrated schematically in Figure 2 for different processes. The depth into the layer increases along the x-axis, with zero representing the upper surface of the layer. Line 8 shows the profile achieved using an implantation process, whilst line 10 shows the profile for a spin-coating, or sputtering process. Implantation results in a peak in the profile occurring within the body of the layer, whereas with the other processes, the highest concentration occurs at the upper surface of the layer. It is thought that this may lead to the formation of better quality crystalline

material in comparison with the other doping techniques, as there is a greater concentration of nickel towards the centre of the body of semiconductor material. The use of implantation also facilitates close control of the nickel dosage. The semiconductor material is crystallised by annealing, preferably in N_2 atmosphere, for around 8 hours at 550°C.

Photolithography, implantation, deposition and etching process steps may then be carried out in a known manner to form a poly-Si TFT structure as shown in Figure 3. The semiconductor material is patterned into a poly-Si island 10, comprising doped source and drain regions 12 and 14, an intrinsic channel region 16 and lightly doped regions 18 and 20 therebetween. A layer of insulating material 22 is deposited over the island 10, with vias 24 and 26 defined therein to allow contact to be made with the source and drain regions 12 and 14, respectively by source and drain terminals 30 and 32. A metal gate electrode 28 is provided over the insulating material layer 22.

It may be particularly advantageous in processes in accordance with the present invention to carry out a plasma hydrogenation process after device fabrication to improve its performance. Typically, this is carried out at around 350°C for about 1 hour.

TFTs made in accordance with the processes described herein having a channel width of 50μm have been found to exhibit a leakage current in the off-state of around $8x10^{-11}$ A at a source-drain voltage of 5V, equivalent to $1.6x10^{-12}$ A/μm, and a mobility of around $20cm^2/Vs$.

The TFT leakage characteristics may be further improved by adopting a fingered channel structure, having 2, 3 or more fingers.

Whilst embodiments of the invention are described herein with reference to silicon material (that is, a-Si and poly-Si), it will be apparent that compound semiconductor films (for example silicon films containing germanium) may be used in accordance with the invention.

It will be appreciated that polycrystalline semiconductor films produced in accordance with the techniques described herein are suitable for use in a wide range of applications in which electronic circuits are formed on substrates which cannot withstand high temperatures such as glass. The films may be

used in the formation of active devices such as TFTs, or passive devices (for example resistors, temperature sensors and piezo-resistors) in circuitry on such substrates. TFTs may be employed in AMLCDs, AMPLEDs, X-ray sensors, fingerprint sensors and the like, in the switching matrices of the devices and/or in integrated circuitry on the same substrate as the switching matrices.

The crystalline quality of polycrystalline semiconductor material made using the processes described herein may be further improved by irradiation of the material with an energy beam. As noted above, it may take a significant period of time to scan an energy beam across a substrate. However, as disclosed in copending United Kingdom Patent Application No. 0211724.0 of the present applicants (our reference PHGB020072), the time taken for this may be minimised in the manufacture of active matrix displays by only irradiating the peripheral circuitry integrated on the display substrate around the display area. The contents of United Kingdom Patent Application No. 0211724.0 are incorporated herein by reference.

From reading the present disclosure, other variations and modifications will be apparent to persons skilled in the art. Such variations and modifications may involve equivalent and other features which are already known in the art, and which may be used instead of or in addition to features already described herein.

Although Claims have been formulated in this Application to particular combinations of features, it should be understood that the scope of the disclosure of the present invention also includes any novel feature or any novel combination of features disclosed herein either explicitly or implicitly or any generalisation thereof, whether or not it relates to the same invention as presently claimed in any Claim and whether or not it mitigates any or all of the same technical problems as does the present invention.

The Applicants hereby give notice that new Claims may be formulated to such features and/or combinations of such features during the prosecution of the present Application or of any further Application derived therefrom.

CLAIMS

1. An electronic device comprising a TFT, the TFT including a channel defined in a layer of polycrystalline semiconductor material produced by crystallising amorphous semiconductor material using metal atoms to promote the crystallisation process, wherein the semiconductor material includes an average concentration of metal atoms in the range $1.3x10^{18}$ to $7.5x10^{18}$ atoms/cm^3.

2. An electronic device of Claim 1 wherein the average concentration of metal atoms in the semiconductor material is around $2.5x10^{18}$ atoms/cm^3.

3. A method of manufacturing an electronic device including the steps of:

(a) depositing amorphous semiconductor material on a substrate;

(b) adding metal atoms to the semiconductor material at an average concentration therein in the range $1.3x10^{18}$ to $4x10^{18}$ atoms/cm^3, the metal atoms being suitable for accelerating the crystallisation of amorphous semiconductor material; and

(c) annealing the amorphous semiconductor material to form polycrystalline semiconductor material.

4. A method of Claim 3 wherein the metal atoms are added to the amorphous semiconductor material at an average concentration therein of around $2.5x10^{18}$ atoms/cm^3.

5. A method of Claim 3 or Claim 4 wherein the metal atoms are added by implantation.

6. A method of any of Claims 3 to 5 wherein the annealing process is carried out for 10 hours or less at a temperature of 600°C or less, and a TFT

is formed with its channel defined in the polycrystalline semiconductor material which exhibits a minimum leakage current of around $2.5x10^{-12}$ A/μm or less at a source-drain voltage of 5V.

7. A method of Claim 6 wherein the annealing process is carried out for 8 hours or less at a temperature of 550°C or less, and a TFT is formed with its channel defined in the polycrystalline semiconductor material which exhibits a minimum leakage current of around $2.5x10^{-12}$ A/μm or less at a source-drain voltage of 5V.

8. An electronic device of Claim 1 or Claim 2 or a method of any of Claims 3 to 7 wherein the metal atoms comprise nickel atoms.

9. An electronic device substantially as described herein with reference to the accompanying Drawings.

10. A method of manufacturing an electronic device substantially as described herein with reference to the accompanying Drawings.

ABSTRACT

ELECTRONIC DEVICES AND THEIR MANUFACTURE

An electronic device comprises a thin film transistor (TFT), the TFT including a channel (16) defined in a layer of polycrystalline semiconductor material (10). The polycrystalline semiconductor material is produced by crystallising amorphous semiconductor material (2) using metal atoms (6) to promote the crystallisation process. The polycrystalline semiconductor material (10) includes an average concentration of metal atoms in the range $1.3x10^{18}$ to $7.5x10^{18}$ atoms/cm^3. This enables polycrystalline semiconductor TFTs to be formed with leakage properties acceptable for use in active matrix displays using a metal induced crystallisation process of duration significantly less that previously thought necessary.

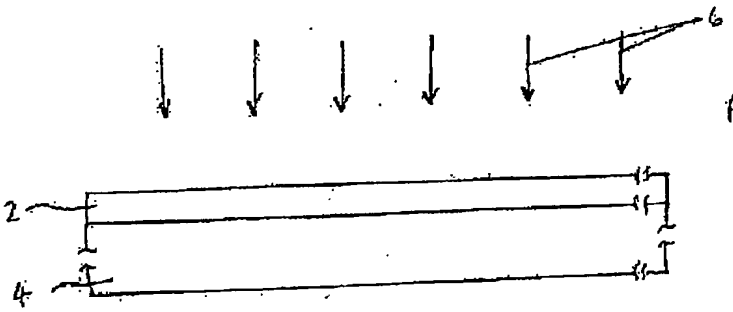

Fig. 1

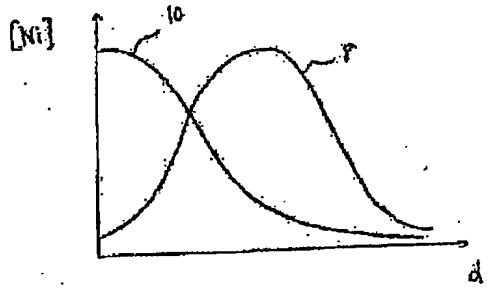

Fig. 2

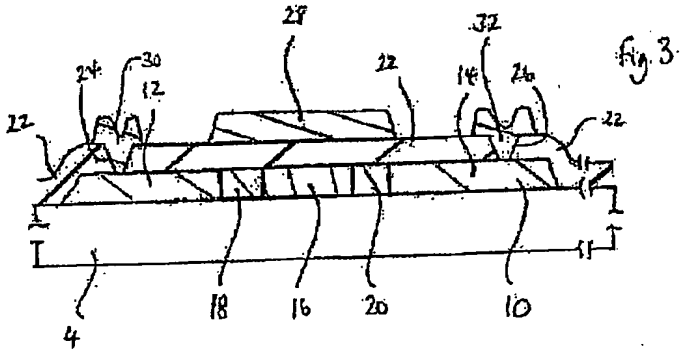

Fig. 3

PHGB 020109